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THE CHINESE UNIVERSITY OF HONG KONG

Department of Information Engineering

Seminar

High-Bandwidth Systems for Data Analytics, HPC, and Machine Learning

By

Prof Peter Hofstee

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Date : 2nd April, 2019 (Tue)
Time : 4:30pm – 6:00pm
Venue : Room 801, Ho Sin Hang Engineering Building
The Chinese University of Hong Kong

Abstract

While performance per dollar (and per Watt) of conventional processors is no longer improving at the rate we enjoyed for three decades, bandwidth per dollar is still improving rapidly. In our talk, we show how these improvements in bandwidth (both for storage and I/O), combined with more specialized computational elements like GPUs and FPGAs can help us achieve significant performance improvements on a broad range of applications. We will show the benefits on applications ranging from database analytics to HPC and ML/DL. We use OpenPOWER systems based on the bandwidth-intensive IBM POWER9 processors for our examples. We also intend to spend time on more optimized programming interfaces, and specifically we will take a deeper look at work done in my group at TU Delft to make it easier to program FPGAs with good performance by building on the Apache Arrow in-memory format and leveraging the shared memory accelerated architectures that POWER9 and its "CAPI" interfaces enable.

Biography

Harm Peter Hofstee is a Dutch physicist and computer scientist who currently is a distinguished research staff member at the IBM Austin Research Laboratory, USA, and a part-time professor in Big Data Systems at Delft University of Technology, Netherlands. Hofstee was born in Groningen and obtained his master's degree in theoretical physics of the University of Groningen in 1988. He continued to study at the California Institute of Technology where he wrote a master's thesis Constructing Some Distributed Programs in 1991 and obtained a Ph.D. with a thesis titled Synchronizing Processes in 1995. He joined Caltech as a lecturer for two years and moved to IBM in the Austin, Texas, Research Laboratory, where he had staff member, senior technical staff member and distinguished engineer positions.

Hofstee is best known for his contributions to Heterogeneous computing as the chief architect of the Synergistic Processor Elements in the Cell Broadband Engine processor used in the Sony PlayStation 3, and the first supercomputer to reach sustained Petaflop operation. After returning to IBM research in 2011 he has focused on optimizing the system roadmap for big data, analytics, and cloud, including the use of accelerated compute. His early research work on coherently attached reconfigurable acceleration on POWER7 paved the way for the new coherent attach processor interface on POWER8. Hofstee is an IBM Master Inventor with more than 100 issued patents and a member of the IBM Academy of Technology.

**** ALL ARE WELCOME ****

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